AMENDMENTS TO THE CLAIMS:

Please amend the Claims as follows:

1. (Currently Amended) A test apparatus for testing a semiconductor device, comprising:

an external test unit;

a built in self test (BIST) circuit formed in the semiconductor device; and

a built out self test (BOST) device which is coupled between the external test unit and the semiconductor device, wherein first pattern data for a pattern dependency test is previously stored in the BIST circuit and second pattern data for a timing dependency test is previously stored in the BOST device, wherein the BOST device includes

a pattern generating circuit, coupled to the semiconductor device, for providing the previously stored second pattern data for the timing dependency test to the semiconductor device, and

a decision circuit, coupled to the pattern generating circuit and the semiconductor device, for receiving test data originating from the second pattern data from the semiconductor device and determining the test result of the timing dependency test using the test data and the second pattern data,

wherein the pattern generating circuit includes

a pattern memory for storing the second pattern data for the timing dependency test,

a timing generator, coupled to the pattern memory, for generating a reference clock signal and receiving the second pattern data for the timing dependency test from the pattern memory, and

a wave formatter, coupled to the timing generator, for receiving the second pattern data for the timing dependency test from the timing generator in accordance with the reference clock signal and providing the second pattern data for the timing dependency test to the semiconductor device as front pattern data, wherein the wave formatter generates back pattern data by inverting the front pattern data in accordance with a control signal,

wherein the decision circuit includes a measuring circuit for measuring an access time of the semiconductor device using an output signal from the semiconductor device and the clock signal output from the pattern generating circuit, and

wherein the measuring circuit includes:

a logic circuit for generating an EOR logical signal by performing an EOR operation on the clock signal and the output signal; and

a frequency counter, coupled to the logic circuit, for measuring a time interval of the EOR logical signal.

2. (Canceled)

3. (Canceled)

4. (Previously Presented) The test apparatus according to claim 1, wherein the external test unit provides the BOST device with an output level generating voltage which is used to generate an output level and a reference voltage for input level decision, which is used to determine an input signal supplied from the BOST device.

5. (Previously Presented) The test apparatus according to claim 1, wherein the BIST circuit generates a signal indicative of a test result by performing a pattern dependency test on the semiconductor device using the first pattern data for the pattern dependency test, and the decision circuit receives the signal indicative of the test result from the BIST circuit and determines whether the pattern dependency test result is accurate.

6. (Previously Presented) The test apparatus according to claim 1, wherein based on a determination result on the test result of the timing dependency test, the decision circuit provides reference data to the external test unit or generates inverted data of the reference data and provides the inverted data to the external test unit.

7. (Previously Presented) The test apparatus according to claim 1, wherein the semiconductor device is one of a plurality of semiconductor devices arranged on a wafer, and the test apparatus further comprises:

a contactor substrate for coupling the BOST device to the semiconductor device; and

a switch circuit, provided in the contactor substrate, for disconnecting the BOST device from the semiconductor device in accordance with a determination result from the decision circuit.

8. (Previously Presented) The test apparatus according to claim 1, wherein the semiconductor device is one of a plurality of semiconductor devices arranged on a wafer, the BOST device has a first surface having a first contactor, which is coupled to the semiconductor device, and a second surface having a second contactor, and the test apparatus further comprises a contactor substrate coupled to the second contactor.

9. (Canceled)

10. (Previously Presented) The test apparatus according to claim 1, wherein the semiconductor device is one of a plurality of semiconductor devices arranged on a wafer, and the test apparatus further comprises:

a socket for retaining the BOST device; and

a contactor substrate, applied to the socket, for connecting the BOST device to the semiconductor device.

11. (Currently Amended) The test apparatus according to claim 1, wherein the pattern generating circuit generates a the clock signal, and the test apparatus further comprises:

a first interconnection line for supplying the clock signal to the semiconductor device from the pattern generating circuit;

a second interconnection line for connecting the semiconductor device to the decision circuit; and

a third interconnection line which has a length equal to a sum of lengths of the first and second interconnection lines and provides the clock signal to the decision circuit from the pattern generating circuit.

12. (Canceled)

13. (Canceled)

14. (Currently Amended) ~~The~~ A test apparatus ~~according to claim 12~~ for testing a semiconductor, comprising:

an external test unit;

a built in self test (BIST) circuit formed in the semiconductor device; and

a built out self test (BOST) device which is coupled between the external test unit and the semiconductor device, wherein first pattern data for a pattern dependency test is previously stored in the BIST circuit and second pattern data for a timing dependency test is previously stored in the BOST device, wherein the BOST device includes

a pattern generating circuit, coupled to the semiconductor device, for providing the previously stored second pattern data for the timing dependency test to the semiconductor device, and

a decision circuit, coupled to the pattern generating circuit and the semiconductor device, for receiving test data originating from the second pattern data from the semiconductor device and determining the test result of the timing dependency test using the test data and the second pattern data,

wherein the pattern generating circuit includes

a pattern memory for storing the second pattern data for the timing dependency test,

a timing generator, coupled to the pattern memory, for generating a reference clock signal and receiving the second pattern data for the timing dependency test from the pattern memory, and

a wave formatter, coupled to the timing generator, for receiving the second pattern data for the timing dependency test from the timing generator in accordance with the reference clock signal and providing the second pattern data for the timing dependency test to the semiconductor device as front pattern data, wherein the wave formatter generates back pattern data by inverting the front pattern data in accordance with a control signal,

wherein the decision circuit includes a measuring circuit for measuring an access time of the semiconductor device using an output signal from the semiconductor device and a clock signal output from the pattern generating circuit,

wherein the measuring circuit includes:

an OR circuit for receiving an output signal of plural bits output from the semiconductor device and generating an OR logical signal;

an AND circuit for receiving an output signal of plural bits output from the semiconductor device and generating an AND logical signal;

a first frequency counter, coupled to the OR circuit, for generating a first count value in accordance with the OR logical signal and the clock signal;

a second frequency counter, coupled to the AND circuit, for generating a second count value in accordance with the AND logical signal and the clock signal; and

an access-time measuring circuit, coupled to the first and second frequency counters, for measuring an access time of the semiconductor device based on one of the first and second count values.

15. (Canceled)